CLAIMS

1. (Previously presented) A device, comprising:

a splitter adapted to receive an input signal and generate a first copy and a second copy of the input signal;

a first comparator adapted to receive the first copy of the input signal and generate a first binary signal;

a second comparator adapted to receive the second copy of the input signal and generate a second binary signal; and

a logic gate adapted to generate a third binary signal based on the first and second binary signals, wherein:

the input signal corresponds to a duobinary sequence; and

the third binary signal is a binary representation of the duobinary sequence.

2. (Original) The device of claim 1, wherein the input signal is an analog signal.

3. (Original) The device of claim 1, wherein the logic gate comprises an exclusive-OR gate.

4. (Canceled)

5. (Previously presented) The device of claim 1, wherein the splitter has a bandwidth of at least about $1/2T_b$, where T_b is a bit period corresponding to the input signal.

6. (Original) The device of claim 5, wherein each of the first and second comparators and the logic gate has a bandwidth of about $1/T_b$.

7. (Original) The device of claim 1, wherein the input signal corresponds to a bit rate of higher than about 10 Gb/s.

8. (Original) The device of claim 1, wherein:

for each comparator,

when voltage applied to a first input port is equal to or higher than voltage applied to a second input port, the corresponding binary signal has binary "0"; and

when the voltage applied to the first input port is lower than the voltage applied to the second input port, the corresponding binary signal has binary "1".

9. (Original) The device of claim 8, wherein:

for the first comparator,

the first copy is applied to the first input port; and

a first threshold voltage is applied to the second input port; and

for the second comparator,

a second threshold voltage is applied to the first input port; and

the second copy is applied to the second input port.

10. (Original) The device of claim 9, wherein the logic gate is an exclusive-OR gate.

11. (Original) The device of claim 8, wherein:

for each comparator,

a corresponding threshold voltage is applied to the first input port; and

the corresponding signal copy is applied to the second input port.

12. (Original) The device of claim 11, wherein the logic gate is an exclusive-NOR gate.

13. (Original) The device of claim 1, wherein the device is implemented in an integrated circuit.

14. (Previously presented) A method of signal processing, comprising:

(A) comparing magnitude of an electrical signal with first and second threshold voltages to generate first and second binary values;

(B) applying a logic function to the first and second binary values to generate a third binary value; and

(C) repeating steps (A) and (B) to generate a sequence of third binary values, wherein:

step (A) comprises generating a first copy and a second copy of the electrical signal using a splitter;

the electrical signal corresponds to a duobinary sequence; and

the sequence of third values is a binary representation of the duobinary sequence.

15. (Original) The method of claim 14, wherein the logic function comprises an exclusive-OR function.

16. (Original) The method of claim 14, wherein, for step (A):

for each threshold voltage,

when the magnitude of the electrical signal is equal to or higher than the threshold voltage, the corresponding binary value is "0"; and

when the magnitude of the electrical signal is lower than the threshold voltage, the corresponding binary value is "1".

17. (Original) The method of claim 14, wherein, for step (A):

when the magnitude of the electrical signal is equal to or higher than the first threshold voltage, the first binary value is "0";

when the magnitude of the electrical signal is lower than the first threshold voltage, the first binary value is "1";

when the magnitude of the electrical signal is equal to or lower than the second threshold voltage, the second binary value is "0"; and

when the magnitude of the electrical signal is higher than the second threshold voltage, the second binary value is "1".

18. (Previously presented) A data transmission system designed to use duobinary signaling, the system including a device comprising:

a splitter adapted to receive an input signal and generate a first copy and a second copy of the input signal;

a first comparator adapted to receive the first copy of the input signal and generate a first binary signal;

a second comparator adapted to receive the second copy of the input signal and generate a second binary signal; and

a logic gate adapted to generate a third binary signal based on the first and second binary signals, wherein:

the input signal corresponds to a duobinary sequence; and

the third binary signal is a binary representation of the duobinary sequence.

19. (Original) The system of claim 18, further comprising:

an encoder coupled to a transmission channel, wherein:

the encoder is configured to generate the duobinary sequence based on a received binary sequence and apply the duobinary sequence to the transmission channel; and

the transmission channel is configured to apply the input signal to the device.

20. (Original) The system of claim 19, wherein the binary sequence received by the encoder has inter-symbol correlation data.

21. (Previously presented) A device, comprising means for converting an analog duobinary signal into a digital binary signal, wherein:

the means for converting comprises means for generating a first copy and a second copy of the duobinary signal, said means for generating having a bandwidth of at least about $1/2T_b$, where T_b is a bit period corresponding to the duobinary signal;

the first copy is compared with a first threshold voltage;

the second copy is compared with a second threshold voltage; and

the digital binary signal is generated based on results of the comparisons.

22. (Original) The device of claim 21, wherein the means for converting comprises a differential exclusive-OR device.

23. (Previously presented) The device of claim 9, wherein each of the first and second threshold voltages is a selected constant voltage.

24. (Previously presented) The device of claim 9, wherein each of the first and second threshold voltages is not based on peak detection in the input signal.

25. (Previously presented) The device of claim 11, wherein, for each comparator, the threshold voltage is a selected constant voltage.

26. (Previously presented) The device of claim 11, wherein, for each comparator, the threshold voltage is not based on peak detection in the input signal.

27. (Previously presented) The method of claim 14, wherein each of the first and second threshold voltages is a selected constant voltage.

28. (Previously presented) The method of claim 14, wherein each of the first and second threshold voltages is not based on peak detection in the electrical signal.

29. (Currently amended) The ~~device~~ method of claim 14, wherein the splitter has a bandwidth of at least about $1/2T_b$, where T_b is a bit period corresponding to the electrical signal.

30. (Previously presented) The device of claim 18, wherein the splitter has a bandwidth of at least about $1/2T_b$, where T_b is a bit period corresponding to the input signal.

31. (New) A method of signal processing, comprising:

(A) splitting an input signal representing a duobinary sequence into first and second copies using a splitter;

(B) comparing (i) magnitude of the first copy with a first threshold voltage to generate a first binary value and (ii) magnitude of the second copy with a second threshold voltage to generate a second binary value, wherein:

said comparison is performed asynchronously without recovering a clock signal corresponding to the input signal; and

each of the first and second threshold voltages is not based on peak detection in the input signal; and

(C) applying a logic function to the first and second binary values to generate an output signal having a binary representation of the duobinary sequence.

32. (New) A device, comprising:

(A) a splitter adapted to split an input signal representing a duobinary sequence into first and second copies;

(B) means for comparing (i) magnitude of the first copy with a first threshold voltage to generate a first binary value and (ii) magnitude of the second copy with a second threshold voltage to generate a second binary value, wherein:

said comparison is performed asynchronously without recovering a clock signal corresponding to the input signal; and

each of the first and second threshold voltages is not based on peak detection in the input signal; and

(C) means for applying a logic function to the first and second binary values to generate an output signal having a binary representation of the duobinary sequence.